REMARKS / DISCUSSION OF ISSUES

The present amendment is submitted in response to the Office Action mailed September 1, 2009. In view of the amendments above and the remarks to follow, reconsideration and allowance of this application are respectfully requested.

Status of Claims

Claims 1-17 are pending in this application. Claims 1 and 11 are amended.

Interview Summary

Applicants appreciate the courtesy granted to Applicant's attorney, Michael A. Scaturro (Reg. No. 51,356), during a telephonic interview conducted on Wednesday, October 28, 2009. During the informal telephonic interview, a proposed amendment to Claim 1 was discussed with particular reference to the cited reference, Kimura. The Examiner understood and appreciated the Applicants proposals and remarked that the proposed amendment overcomes the Kimura reference, however, a further search will be required necessitating the filing of an RCE.

Claim Rejections under 35 USC 102

In the Office Action, Claims 1-4, 6, 8-13 and 15-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application No. 2004/0085270 ("Kimura"). Applicants respectfully traverse the rejections.

Claims 1-4, 6 and 8-10 are allowable

The cited portions of Kimura do not anticipate claim 1, because the cited portions of Kimura fail to disclose every element of claim 1. For example, the cited portions of Kimura

fail to disclose or suggest. "*a reference driver circuit (30), outputting a constant reference current that does not change in response to said input data, wherein the reference driver circuit (30) is for dynamically calibrating at least one of the controllable driver circuits whilst the other controllable driver circuits provide inputs to the data conductors, wherein each of said plurality of controllable driver circuits (32, 34, 40) includes a switching block (35) which enables the output of each of said plurality of controllable driver circuits (32, 34, 40)to be connected selectively to the reference driver circuit (30) during a first addressing period to perform a calibration operation and to a respective output of the display device in a further addressing period to perform a driving operation, and wherein the calibration and driving operations for each of said plurality of controllable driver circuits (32, 34, 40) are interchanged during successive addressing periods*", as recited in claim 1. (Emphasis Added).

Kimura discloses a signal-line drive circuit that operates in a different manner than described by the invention. As understood by Applicants, Kimura discloses a signal-line drive circuit that operates according to a current input method in which drain current is set to have the same value as that of the signal current set in the current source circuit. This is described in Kimura at par. 17.

[0017] As described above, the current input method refers to a method in which the drain current of the TFT 609 is set to have the same current value as that of the signal current I_{data} set in the current source circuit 612, and the light emitting element 611 emits light with the luminance corresponding to the drain current. By using the thus structured pixel, the effects of the characteristic variations of TFTs constituting the pixel is reduced, and a desired current can be supplied to the light emitting element.

A key feature of the invention is the reduction in the spread of driver circuit outputs by calibration of the driver circuits using a reference driver circuit. The reference driver circuit comprises a **constant reference current source**. Each driver circuit includes **a dedicated switching block** which enables the particular driver circuit's output to be selectively connected to the constant reference current source or to the output of the display device. **The calibration and driving operations for each of the driver circuits are interchanged during successive addressing periods.**

In contrast to claim 1, Kimura discloses that a video signal 109 (i.e., reference driver circuit 30, Iref) outputs a variable reference current that **changes in response to the input data**. This feature of Kimura is admitted by the Office at page 2 of the Office Action, "*video signal driver 109 which inherently changes based upon the video signal to be supplied to the driver circuits.*" Claim 1 has been amended in relevant part to recite that the invention does not claim a current source that changes in response to the input data. Instead, the invention discloses a reference driver circuit 30, Iref, that outputs a **constant reference current** that **does not change in response to the input data**.

Further, Kimura discloses that the video signal 109 is connected to an **input** of the driver circuits, as illustrated in Figure 4. In contrast to Kimura, the constant reference driver circuit 30 of the invention is connected to an **output** of the driver circuits. Claim 1 recites in relevant part, "*a reference driver circuit (30), outputting a constant reference current that does not change in response to said input data.*"

Further, Kimura **does not disclose** that **the calibration and driving operations are interchanged during successive addressing periods**. Instead, as stated above, Kimura discloses a signal-line drive circuit that operates according to a current input method in which drain current is set to have the same value as that of the signal current set in the current source circuit. See Kimura, par. 17. It is respectfully submitted that **the current input method of Kimura does not operate by interchanging calibration and driving operations during successive addressing periods**. Instead, the current input method of Kimura operates by setting a drain current of the TFT to have the same current value as that of the signal current I_{data} set in the current source. In this manner, light is emitted with a luminance corresponding to the drain current. In contrast to Kimura, the invention discloses a reference driver circuit comprising a reference current source that dynamically calibrates driver circuits so as to reduce the spread in the output of current source circuits. As described in Applicant's specification at pages 9-10, and illustrated in Fig. 3, **during a first time period**, a first current source 32 (I_{cal}), **is adjusted** to draw exactly the same current (I_{ref}) as the constant reference current source 30. During this first time period, while current source 32 is being **dynamically calibrated** by means of the adjustment, the other current source 34, delivers the output

current (I_{out}) to activate the pixel in the single column. Thereafter, **during a second time period**, the two current sources are **interchanged**, and while current source 34 is being dynamically calibrated, in the manner described above, current source 32 delivers the output current.

Based on the foregoing, it is respectfully submitted that claim 1 is allowable.

Claims 2-4 and 8-10 depend from claim 1, which Applicant has shown to be allowable. Hence the cited portions of Kimura fail to disclose or suggest at least one element of each of claims 2-4 and 8-10. Accordingly, claims 2-4 and 8-10 are also allowable, at least by virtue of their dependence from claim 1.

Claims 11-13 and 15-17 are allowable

Independent Claim 11 recites similar subject matter as Independent Claim 1 and therefore contains the limitations of Claim 1. Hence, for at least the same reasons given for Claim 1, Claim 11 is believed to recite statutory subject matter under 35 USC 102(e).

Claims 12-13 and 15-17 depend from claim 11, which Applicant has shown to be allowable. Hence the cited portions of Kimura fail to disclose or suggest at least one element of each of claims 12-13 and 15-17. Accordingly, claims 12-13 and 15-17 are also allowable, at least by virtue of their dependence from claim 11.

Claim Rejections under 35 USC 103

The Office has rejected claims 5, 7 and 14 under 35 U.S.C. §103(a), as being unpatentable over Kimura. Applicant respectfully traverses the rejections.

Claims 5, 7 and 14 are Allowable

As explained above, Kimura does not disclose or suggest each and every element of claims 1 and 11, from which claims 5, 7 and 14 depend, respectively. Specifically, the cited portions of Kimura fail to disclose or suggest "*a reference driver circuit (30), outputting a*

constant reference current that does not change in response to said input data, wherein the reference driver circuit (30) is for dynamically calibrating at least one of the controllable driver circuits whilst the other controllable driver circuits provide inputs to the data conductors, wherein each of said plurality of controllable driver circuits (32, 34, 40) includes a switching block (35) which enables the output of each of said plurality of controllable driver circuits (32, 34, 40)to be connected selectively to the reference driver circuit (30) during a first addressing period to perform a calibration operation and to a respective output of the display device in a further addressing period to perform a driving operation, and wherein the calibration and driving operations for each of said plurality of controllable driver circuits (32, 34, 40) are interchanged during successive addressing periods", as recited in claim 1. (Emphasis Added).

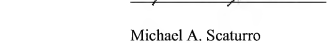
Therefore, Kimura does not disclose each and every element of claims 1 and 11, from which claims 5-7 and 14 depend, respectively. Hence, claims 5-7 and 14 are allowable.

Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-17 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Mike Belk, Esq., Intellectual Property Counsel, Philips Electronics North America, at 914-945-6000.

Respectfully submitted,



Michael A. Scaturro
Reg. No. 51,356
Attorney for Applicant

Mailing Address:
Intellectual Property Counsel
Philips Electronics North America Corp.
P.O. Box 3001
345 Scarborough Road
Briarcliff Manor, New York 10510-8001